

ABSTRACT OF THE DISCLOSURE

A semiconductor device evaluation method and apparatus are provided which do not require a measurer to expend a great deal of time and effort even when measuring a large number of points, can prevent the occurrence of variations in measured values 5 from measurer to measurer, and allow the measurement of the finished gate length even if gate pattern does not appear on the semiconductor device surface. There is also provided a semiconductor device manufacturing control method which applies such an evaluation method and apparatus to the control of semiconductor device manufacturing. For a plurality of insulated gate transistors with different channel lengths, an effective 10 channel length (L_{eff}), a gate capacitance (C_g), and a fringing capacitance (C_f) are determined by electrical measurement and/or calculation. The gate capacitance (C_g) and the effective channel length (L_{eff}) are extended on a graph by extrapolation to determine gate-capacitance-vs.-effective-channel-length characteristics. Then, a gradient (A) of the characteristics is calculated to determine the finished gate length (L_g) for each of the 15 plurality of insulated gate transistors from the equation, $L_g = (C_g - C_f)/A$.